**Design the memory map and memory decoder for a 16 bits microprocessor system using the following memory requirements:**

**- 256KB EEPROM ending at FFFFFH, using 64K x 16 bits memories**

**- 128KB DRAM, using 32K x 8 bits memories**

**STEP 1**

**STEP 2**

**STEP 3**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| ***BLOCK*** | ***BLOCK SIZE*** | ***ADDRESS LINES*** | ***ADDRESS RANGE*** | |
| B1 | 128 KB | 17 | 0x0\_0000 | 0x1\_FFFF |
| B2 | 128 KB | 17 | 0x0\_0000 | 0x1\_FFFF |
| B3 | 64 KB | 16 | 0x0000 | 0xFFFF |
| B4 | 64 KB | 16 | 0x0000 | 0xFFFF |

**STEP 4**

|  |  |  |
| --- | --- | --- |
| ***TYPE*** | ***BLOCK*** | ***MEMORY MAP*** |
| DRAM | B3 | 0x0\_0000 |
| 0x0\_FFFF |
| B4 | 0x1\_0000 |
| 0x1\_FFFF |
| . . . | | |
| EEPROM | B1 | 0xC\_0000 |
| 0xD\_FFFF |
| B2 | 0xE\_0000 |
| 0xF\_FFFF |

**STEP 5**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| ***A19*** | ***A18*** | ***A17*** | ***A16*** | ***A15*** | ***A14*** | ***...*** | ***A1*** | ***A0*** |  |
| 1 | 1 | 0 | 0 | 0 | 0 | ... | 0 | 0 | ***B1*** |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | ***B2*** |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | ***B3*** |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | ***B4*** |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |

**STEP 6**

**STEP 7**



**3-TO-8**

**DECODER**

**B3**

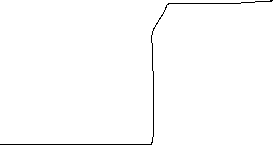
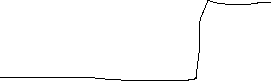
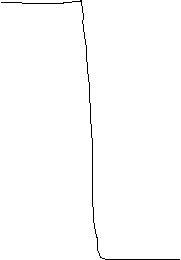
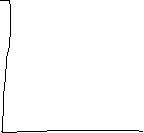
**B4**

**B2**

**B1**



**Design the memory map and memory decoder for a 16 bits microprocessor system using the following memory requirements:**



**- 256KB EEPROM starting at 40000H, using 64K x 8 bits memories**

**- 256KB DRAM, using 64K x 1 bit memories**

**STEP 1**

**STEP 2**

**STEP 3**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| ***BLOCK*** | ***BLOCK SIZE*** | ***ADDRESS LINES*** | ***ADDRESS RANGE*** | |
| B1 | 128 KB | 17 | 0x0\_0000 | 0x1\_FFFF |
| B2 | 128 KB | 17 | 0x0\_0000 | 0x1\_FFFF |
| B3 | 128 KB | 17 | 0x0\_0000 | 0x1\_FFFF |
| B4 | 128 KB | 17 | 0x0\_0000 | 0x1\_FFFF |

**STEP 4**

|  |  |  |
| --- | --- | --- |
| ***TYPE*** | ***BLOCK*** | ***MEMORY MAP*** |
| DRAM | B3 | 0x0\_0000 |
| 0x1\_FFFF |
| B4 | 0x2\_0000 |
| 0x3\_FFFF |
| EEPROM | B1 | 0x4\_0000 |
| 0x5\_FFFF |
| B2 | 0x6\_0000 |
| 0x7\_FFFF |

**STEP 5**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| ***A19*** | ***A18*** | ***A17*** | ***A16*** | ***A15*** | ***A14*** | ***...*** | ***A1*** | ***A0*** |  |
| 0 | 0 | 0 | 0 | 0 | 0 | ... | 0 | 0 | ***B3*** |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | ***B4*** |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | ***B1*** |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | ***B2*** |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

**STEP 6**

**STEP 7**



**3-TO-8**

**DECODER**

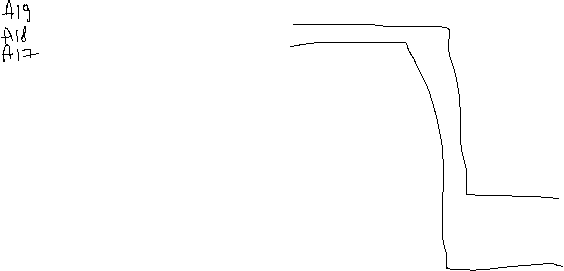
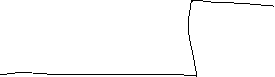
**B3**

**B4**

**B2**

**B1**

**Design the memory map and memory decoder for a 16 bits microprocessor system using the following memory requirements:**



**- 128KB EEPROM, using 64K x 8 bits memories**

**- 512KB DRAM, using 64K x 8 bits memories**

**STEP 1**

**STEP 2**

**STEP 3**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| ***BLOCK*** | ***BLOCK SIZE*** | ***ADDRESS LINES*** | ***ADDRESS RANGE*** | |
| B1 | 128 KB | 17 | 0x0\_0000 | 0x1\_FFFF |
| B2 | 128 KB | 17 | 0x0\_0000 | 0x1\_FFFF |
| B3 | 128 KB | 17 | 0x0\_0000 | 0x1\_FFFF |
| B3 | 128 KB | 17 | 0x0\_0000 | 0x1\_FFFF |
| B3 | 128 KB | 17 | 0x0\_0000 | 0x1\_FFFF |

**STEP 4**

|  |  |  |
| --- | --- | --- |
| ***TYPE*** | ***BLOCK*** | ***MEMORY MAP*** |
| EEPROM | B1 | 0x0\_0000 |
| 0x1\_FFFF |
| DRAM | B2 | 0x2\_0000 |
| 0x3\_FFFF |
| B3 | 0x4\_0000 |
| 0x5\_FFFF |
| B4 | 0X6\_0000 |
| 0x7\_FFFF |
| B5 | 0x8\_0000 |
| 0x9\_FFFF |

**STEP 5**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| ***A19*** | ***A18*** | ***A17*** | ***A16*** | ***A15*** | ***A14*** | ***...*** | ***A1*** | ***A0*** |  |
| 0 | 0 | 0 | 0 | 0 | 0 | ... | 0 | 0 | ***B1*** |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | ***B2*** |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | ***B3*** |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | ***B4*** |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | ***B5*** |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |

**STEP 6**

**STEP 7**



**3-TO-8**

**DECODER**

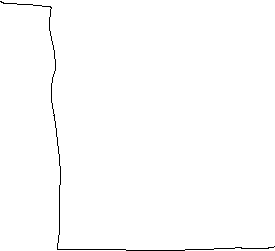
**B3**

**B4**

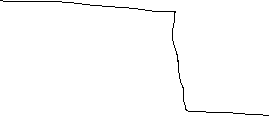
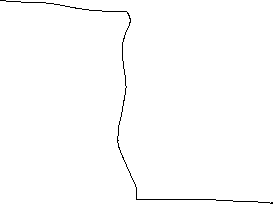
**B2**

**B1**

**Design the memory map and memory decoder for a 16 bits microprocessor system using the following memory requirements:**



**B5**



**- 64KB EEPROM ending at FFFFFH, using 16K x 16 bits memories**

**- 64KB DRAM, starting at 00000h, using 32K x 8 bits memories**

**STEP 1**

**STEP 2**

**STEP 3**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| ***BLOCK*** | ***BLOCK SIZE*** | ***ADDRESS LINES*** | ***ADDRESS RANGE*** | |
| B1 | 32 KB | 15 | 0x0000 | 0x7FFF |
| B2 | 32 KB | 15 | 0x0000 | 0x7FFF |
| B3 | 64 KB | 16 | 0x0000 | 0xFFFF |

**STEP 4**

|  |  |  |
| --- | --- | --- |
| ***TYPE*** | ***BLOCK*** | ***MEMORY MAP*** |
| DRAM | B3 | 0x0\_0000 |
| 0x0\_FFFF |
| . . . | | |
| EEPROM | B1 | 0xF\_0000 |
| 0xF\_7FFF |
| B2 | 0xF\_8000 |
| 0xF\_FFFF |

**STEP 5**

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| ***A19*** | ***A18*** | ***A17*** | ***A16*** | ***A15*** | ***A14*** | ***A13*** | ***A12*** | ***...*** | ***A1*** | ***A0*** |  |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | ... | 0 | 0 | ***B1*** |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | ***B2*** |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | ***B3*** |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |

**STEP 6**

**STEP 7**



**3-TO-8**

**DECODER**

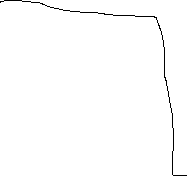
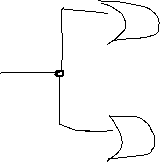
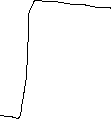
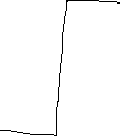
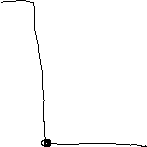
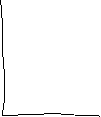
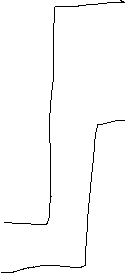
**B3**

**B2**

**B1**



**Design the memory map and memory decoder for a 16 bits microprocessor system using the following memory requirements:**



**- 256KB EEPROM ending at 7ffffH, using 32K x 16 bits memories**

**- 256KB DRAM, using 64K x 8 bits memories**

**STEP 1**

**STEP 2**

**STEP 3**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| ***BLOCK*** | ***BLOCK SIZE*** | ***ADDRESS LINES*** | ***ADDRESS RANGE*** | |
| B1 | 64 KB | 16 | 0x0000 | 0xFFFF |
| B2 | 64 KB | 16 | 0x0000 | 0xFFFF |
| B3 | 64 KB | 16 | 0x0000 | 0xFFFF |
| B4 | 64 KB | 16 | 0x0000 | 0xFFFF |
| B5 | 128 KB | 17 | 0x0\_0000 | 0x1\_FFFF |
| B6 | 128 KB | 17 | 0x0\_0000 | 0x1\_FFFF |

**STEP 4**

|  |  |  |
| --- | --- | --- |
| ***TYPE*** | ***BLOCK*** | ***MEMORY MAP*** |
| DRAM | B5 | 0x0\_0000 |
| 0x1\_FFFF |
| B6 | 0x2\_0000 |
| 0x3\_FFFF |
| EEPROM | B1 | 0x4\_0000 |
| 0x4\_FFFF |
| B2 | 0x5\_0000 |
| 0x5\_FFFF |
| B3 | 0x6\_0000 |
| 0x6\_FFFF |
| B4 | 0x7\_0000 |
| 0x7\_FFFF |

**STEP 5**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| ***A19*** | ***A18*** | ***A17*** | ***A16*** | ***A15*** | ***A14*** | ***...*** | ***A1*** | ***A0*** |  |
| 0 | 0 | 0 | 0 | 0 | 0 | ... | 0 | 0 | ***B5*** |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | ***B6*** |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | ***B1*** |
| 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | ***B2*** |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | ***B3*** |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | ***B4*** |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

**STEP 6**

**STEP 7**

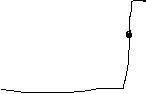
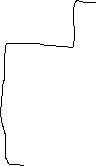
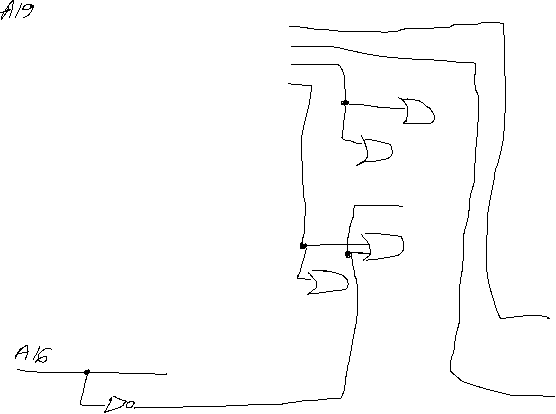
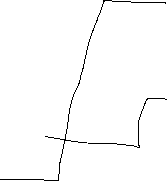
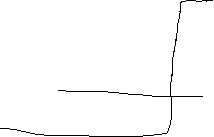
**B1**



**3-TO-8**

**DECODER**

**Design the memory map and memory decoder for a 16 bits microprocessor system using the following memory requirements:**



**B6**

**B5**

**B4**

**B3**

**B2**



**- 192KB EEPROM, using 32K x 16 bits memories**

**- 128KB DRAM, using 32K x 8 bits memories**

**STEP 1**

**STEP 2**

**STEP 3**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| ***BLOCK*** | ***BLOCK SIZE*** | ***ADDRESS LINES*** | ***ADDRESS RANGE*** | |
| B1 | 64 KB | 16 | 0x0000 | 0xFFFF |
| B2 | 64 KB | 16 | 0x0000 | 0xFFFF |
| B3 | 64 kb | 16 | 0x0000 | 0xFFFF |
| B4 | 64 KB | 16 | 0x0000 | 0xFFFF |
| B5 | 64 KB | 16 | 0x0000 | 0xFFFF |

**STEP 4**

|  |  |  |
| --- | --- | --- |
| ***TYPE*** | ***BLOCK*** | ***MEMORY MAP*** |
| EEPROM | B1 | 0x0\_0000 |
| 0x0\_FFFF |
| B2 | 0x1\_0000 |
| 0x1\_FFFF |
| DRAM | B3 | 0x2\_0000 |
| 0X2\_FFFF |
| B4 | 0x3\_0000 |
| 0x3\_FFFF |
| B3 | 0x4\_0000 |
| 0X4\_FFFF |

**STEP 5**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| ***A19*** | ***A18*** | ***A17*** | ***A16*** | ***A15*** | ***A14*** | ***...*** | ***A1*** | ***A0*** |  |
| 0 | 0 | 0 | 0 | 0 | 0 | ... | 0 | 0 | ***B1*** |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | ***B2*** |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | ***B3*** |
| 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | ***B4*** |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | ***B5*** |
| 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 |

**STEP 6**

**STEP 7**



**3-TO-8**

**DECODER**

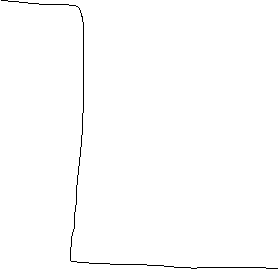
**B3**

**B4**

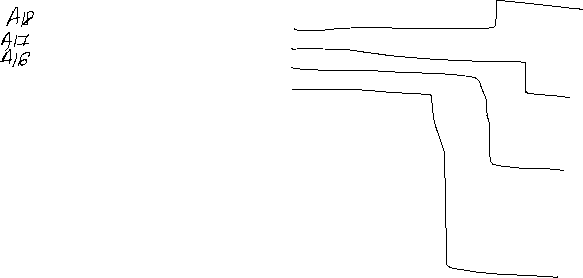
**B2**

**B1**

**Design the memory map and memory decoder for a 16 bits microprocessor system using the following memory requirements:**



**B5**



**- 96KB EEPROM ending at FFFFFH, using 16K x 16 bits memories**

**- 128KB DRAM, using 64K x 2 bits memories**

**STEP 1**

**STEP 2**

**STEP 3**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| ***BLOCK*** | ***BLOCK SIZE*** | ***ADDRESS LINES*** | ***ADDRESS RANGE*** | |
| B1 | 32 KB | 15 | 0x0000 | 0x7FFF |
| B2 | 32 KB | 15 | 0x0000 | 0x7FFF |
| B3 | 32 KB | 15 | 0x0000 | 0x7FFF |
| B4 | 128 KB | 17 | 0x0\_0000 | 0x1\_FFFF |

**STEP 4**

|  |  |  |
| --- | --- | --- |
| ***TYPE*** | ***BLOCK*** | ***MEMORY MAP*** |
| DRAM | B4 | 0x0\_0000 |
| 0x1\_FFFF |
| . . . | | |
| EEPROM | B1 | 0xE\_8000 |
| 0xE\_FFFF |
| B2 | 0xF\_0000 |
| 0xF\_7FFF |
| B3 | 0xF\_8000 |
| 0xF\_FFFF |

**STEP 5**

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| ***A19*** | ***A18*** | ***A17*** | ***A16*** | ***A15*** | ***A14*** | ***A13*** | ***A12*** | ***...*** | ***A1*** | ***A0*** |  |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | ... | 0 | 0 | ***B4*** |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | ***B1*** |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | ***B2*** |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | ***B3*** |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

**STEP 6**

**STEP 7**



**3-TO-8**

**DECODER**

**B3**

**B4**

**B2**

**B1**

